REMARKS

The present application was filed on August 19, 2003 with claims 1 through 28. Claims 1 through 28 are presently pending in the above-identified patent application. Claims 1 and 14 are proposed to be amended herein.

In the Office Action, the Examiner objected to claims 1 and 14 due to indicated informalities. The Examiner rejected claims 1-8, 13, 20, 21, 23, and 24 under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. (United States Patent Application Publication Number 2002/0167282A1) in view of Jania et al. (United States Patent Number 3,575,256), rejected claims 9 and 25 under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of Wu et al., "Bipolar Bootstrapped Multi-emitter BiCMOS Logic for Low-Voltage Applications, Electronics, Circuits, and Systems," 1996, Volume 2, Pages 1174-1177, rejected claim 10 under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of Chur (United States Patent Number 5,124,849), rejected claim 11 under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al., Jania et al., and Chur, and further in view of Ohie et al. (United States Patent Number 5,936,448), rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al., Jania et al., Chur, and Ohie et al., and further in view of Burns et al. (United States Patent Number 4,698,587), rejected claims 14-18 under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of Bassett et al. (United States Patent Number 5,127,008), rejected claims 19 and 22 under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of Kolanek (United States Patent Application Publication Number 2002/0047745 A1), rejected claim 26 under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of Chur and Ohie et al., rejected claim 27 under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of Iida et al. (United States Patent Number 6,525,585), and rejected claim 28 under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. in view of Jania et al., and Takahashi (United States Patent Number 6,253,358).

Formal Objections

Claims 1 and 14 were objected to due to indicated informalities. Regarding claim 1, the Examiner asserts that the recitation of "I method" should be "A method." Regarding claim 14, the Examiner asserts that the phrase "step performing" should be "step of performing."

Claims 1 and 14 have been amended to address the Examiner's concerns and Applicants respectfully request that the objections to claims 1 and 14 be withdrawn.

Independent Claims 1, 20 and 28

Independent claims 1 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. in view of Jania et al., and claim 28 was rejected under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. in view of Jania et al., and Takahashi. Regarding claim 1, the Examiner asserts that Kirkpatrick teaches "one or more performance parameters correlated with maximum operating frequency of one or more electronic components of the electronic system; and adjusting an operating frequency of the one or more electronic components from the electronic system in accordance with the one or more performance parameters" (page 7, paragraph 122; page 39, paragraphs 761, 764). The Examiner acknowledges that Kirkpatrick does not explicitly teach the specific use of determining, at a particular age of the electronic system, one or more performance parameters for the electronic system, but asserts that Jania et al., in an analogous art, teach "system performance of changes in the device parameters with temperature, age and supply voltage" (col. 25, lines 73-75).

Applicants note that, in the text cited by the Examiner, Kirkpatrick teaches that

> an RF control circuit for a lamp includes one or more of the following features: providing a control signal in accordance with input signals representative of forward and reflected power; a method of starting and operating a lamp which includes one or more of the following features: delay of initiation of active control until after the oscillator starts; *stepping an operating frequency of the oscillator through a range of frequencies* ***to find a resonant frequency***; and *adjusting an operating frequency of the oscillator to keep reflected power below a pre-determined threshold.*
> (Paragraph 0122; emphasis added.)

As the Examiner acknowledges, Kirkpatrick does not explicitly teach the specific use of determining, at a particular age of the electronic system, one or more performance parameters for the electronic system. Thus, contrary to the Examiner's assertion, Kirkpatrick does not disclose or suggest ***adjusting an operating frequency of the one or more electronic components*** from the electronic system *in accordance with the one or more performance parameters, wherein the one or more performance parameters are* ***correlated with maximum operating frequency of one or more electronic components of the electronic system for the particular age of the electronic system***.

In addition, Applicants note that, in the text cited by the Examiner, Jania teaches that, "this nulling loop concept of ***setting speed*** *minimizes effects on system performance of changes in the device parameters with temperature, age and supply voltage*." (Col. 25, lines 72-75 emphasis added.) Jania does not disclose or suggest, however, performance parameters ***correlated with maximum operating frequency*** *of one or more electronic components of the electronic system* ***for the particular age of the electronic system.*** Independent claims 1, 20, and 28, as amended, require determining, at a particular age of the electronic system, one or more performance parameters for the electronic system, the one or more performance parameters correlated with maximum operating frequency of one or more electronic components of the electronic system for the particular age of the electronic system; and adjusting an operating frequency of the one or more electronic components from the electronic system in accordance with the one or more performance parameters.

Thus, Kirkpatrick et al. and Jania et al., alone or in combination, do not disclose or suggest determining, at a particular age of the electronic system, one or more performance parameters for the electronic system, the one or more performance parameters correlated with maximum operating frequency of one or more electronic components of the electronic system for the particular age of the electronic system; and adjusting an operating frequency of the one or more electronic components from the electronic system in accordance with the one or more performance parameters, as required by independent claims 1, 20, and 28, as amended.

Additional Cited References

Wu et al. was also cited by the Examiner for its disclosure to compare speed performance of the new BiCMOS logic circuit with those of CMOS, conventional BiCMOS, and Bootstrapped BiCMOS logic circuits (Abstract).

Applicants note that Wu et al. is directed to the bipolar bootstrapped multi-emitter BiCMOS logic and to HSPICE simulations that compare the BiCMOS logic circuit with those of CMOS, conventional BiCMOS, and Bootstrapped BiCMOS logic circuits. Wu et al. do not address the issue of determining, at a particular age of an electronic system, one or more performance parameters for the electronic system, wherein the one or more performance parameters are correlated with a maximum operating frequency of electronic components of the electronic system for the particular age of the electronic system; and adjusting an operating frequency of the electronic components in accordance with the one or more performance parameters.

Chur was also cited by the Examiner for its disclosure of the testing of completed head disk assemblies (HDA) ...develop into a problem as the HAD ages.

Applicants note that Chur is directed to a method for detecting aberrations in a digital data storage medium, such as a magnetic media disk. (See, Abstract.) Chur does not address the issue of determining, at a particular age of an electronic system, one or more performance parameters for the electronic system, wherein the one or more performance parameters are correlated with a maximum operating frequency of electronic components of the electronic system for the particular age of the electronic system; and adjusting an operating frequency of the electronic components in accordance with the one or more performance parameters.

Ohie et al. was also cited by the Examiner for its disclosure of decreasing the noise supply by lowering the operating frequency while threshold voltages are measured to reduce measuring errors.

Applicants note that Ohie et al. is directed to an integrated circuit in which Schmitt input circuits can be tested in a short time and a highly accurate test result can be obtained. (See, Abstract.) Ohie et al. do not address the issue of determining, at a particular age of an electronic system, one or more performance parameters for the electronic system, wherein the one or more performance parameters are correlated with a

maximum operating frequency of electronic components of the electronic system for the particular age of the electronic system; and adjusting an operating frequency of the electronic components in accordance with the one or more performance parameters.

Burns et al. was also cited by the Examiner for its disclosure of determining the maximum operating frequency for which the integrated circuit operates correctly (no logic errors).

Applicants note that Burns et al. is directed to a method for characterizing critical timing paths and analyzing timing related failure modes in high clock rate photocurrent at the drain of a single transistor in a very large scale integrated circuit. (See, Abstract.) Burns et al. do not address the issue of determining, at a particular age of an electronic system, one or more performance parameters for the electronic system, wherein the one or more performance parameters are correlated with a maximum operating frequency of electronic components of the electronic system for the particular age of the electronic system; and adjusting an operating frequency of the electronic components in accordance with the one or more performance parameters.

Bassett et al. was also cited by the Examiner for its disclosure that the second module testing process is performed when it is necessary to enhance the operational reliability of shipped modules, by accelerating and provoking the immediate failure of those correctly but marginally fabricated devices and modules which would otherwise fail early in their expected operational lifespan.

Applicants note that Bassett et al. is directed to a method and apparatus for designing very large scale integrated circuit devices, most particularly level sensitive scan design (LSSD) devices, by inclusion of a plurality of distributed delay lines originating at input terminals of the device, and controlling the inhibiting and enabling of driver circuits connected to the output terminals of the device, as required to regulate operation of device drivers during a plurality of testing operations. (See, Abstract.) Bassett et al. do not address the issue of determining, at a particular age of an electronic system, one or more performance parameters for the electronic system, wherein the one or more performance parameters are correlated with a maximum operating frequency of electronic components of the electronic system for the particular age of the electronic system; and

adjusting an operating frequency of the electronic components in accordance with the one or more performance parameters.

Kolanek was also cited by the Examiner for its disclosure of the set of desired or set point values for the performance parameters, which are provided to the SLMC 320 from some external source such as a wireless communication network system operator.

Applicants note that Kolanek is directed to a signal level and gain management scheme wherein variable internal gain elements are introduced into the LINC amplifier structure in order to maintain internal signal levels at predetermined levels (e.g. optimum signal levels, such as, for example, an optimum SNR) while at the same time permit control of the net gain of the LINC amplifier. (See, paragraph 0014.) Kolanek does not address the issue of determining, at a particular age of an electronic system, one or more performance parameters for the electronic system, wherein the one or more performance parameters are correlated with a maximum operating frequency of electronic components of the electronic system for the particular age of the electronic system; and adjusting an operating frequency of the electronic components in accordance with the one or more performance parameters.

Iida et al. was also cited by the Examiner for its disclosure that the clock generation circuit...manufacture (FIG. 6; col. 3, lines 52-61).

Applicants note that Iida et al. is directed to a fixed-length delay generation circuit designed to restrain variations in delay values caused by, for example, temperature variations. (Col. 1, lines 7-11.) Iida et al. do not address the issue of determining, at a particular age of an electronic system, one or more performance parameters for the electronic system, wherein the one or more performance parameters are correlated with a maximum operating frequency of electronic components of the electronic system for the particular age of the electronic system; and adjusting an operating frequency of the electronic components in accordance with the one or more performance parameters.

Takahashi was also cited by the Examiner for its disclosure that a computer-readable medium...performs the steps. (Col. 18, lines 60-64.)

Applicants note that Takahashi is directed to a method for supporting the design of the semiconductor integrated circuit for the prediction of the performance of a large-scale integrated circuit (LSI) and a system using the same method. (Col. 1, lines 7-14.) Takahashi does not address the issue of determining, at a particular age of an electronic system, one or more performance parameters for the electronic system, wherein the one or more performance parameters are correlated with a maximum operating frequency of electronic components of the electronic system for the particular age of the electronic system; and adjusting an operating frequency of the electronic components in accordance with the one or more performance parameters.

Thus, Wu et al., Chur, Ohie et al., Burns et al., Bassett et al., Kolanek, Iida et al., and Takahashi, alone or in combination, do not disclose or suggest determining, at a particular age of the electronic system, one or more performance parameters for the electronic system, the one or more performance parameters correlated with maximum operating frequency of one or more electronic components of the electronic system for the particular age of the electronic system; and adjusting an operating frequency of the one or more electronic components from the electronic system in accordance with the one or more performance parameters, as required by independent claims 1, 20, and 28, as amended.

<u>Dependent Claims 2-19 and 21-27</u>

Dependent claims 2-8, 13, 21, 23, and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. in view of Jania et al., claims 9 and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of Wu et al., claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of Chur, claim 11 was rejected under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al., Jania et al., and Chur, and further in view of Ohie et al., claim 12 was rejected under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al., Jania et al., Chur, and Ohie et al., and further in view of Burns et al., claims 14-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of Bassett et al., claims 19 and 22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of

Kolanek, claim 26 was rejected under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of Chur and Ohie et al., and claim 27 was rejected under 35 U.S.C. §103(a) as being unpatentable over Kirkpatrick et al. and Jania et al., and further in view of Lida et al.

Claims 2-19 and 21-27 are dependent on claims 1 and 20, respectively, and are therefore patentably distinguished over Kirkpatrick et al., Jania et al., Wu et al., Chur, Ohie et al., Burns et al., Bassett et al., Kolanek, Iida et al., and Takahashi (alone or in any combination) because of their dependency from amended independent claims 1 and 20 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i.e., claims 1-28, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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